The Care and Feeding of High Performance ADCs: Get All the Bits You Paid For

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INTRODUCTION

A new generation of ADCs currently appearing on the scene brings higher performance and lower cost to new markets. Figure 1 shows an example of how high speed 12-bit converters are becoming affordable for the first time to a new range of applications. At the same time, the new converters achieve better dynamic performance with high frequency input signals. This means that more system designers are facing the challenge of using high performance ADCs. In this article, we will talk about some of the problems designers encounter, how to recognize their symptoms and how to avoid them. We will focus on the particular case of the LTC1410, a 1.25Msps, 12-bit ADC. The same considerations become important in higher resolution ADCs at lower speeds. Conversely, lower resolution ADCs will need this same attention at higher speeds.

AN ADC HAS MANY "INPUTS"

Providing a clean analog input signal to an ADC doesn't always guarantee a clean digital output signal. This is because an ADC has not just one input, but many. Ground pins, supply pins and reference pins also act as "inputs" and must be given special care to prevent noise and unwanted signals from corrupting the ADC output. Grounding, bypassing of the supplies and the reference and driving the analog and clock inputs are the major weapons in this battle against corruption.

GROUND PLANES AND GROUNDING

Designing a high speed ADC system without using a proper ground is like trying to play basketball on a huge trampoline. No matter how well you mount the baskets to the court, the whole court will bounce and wobble as the players jump and try to shoot. To play the game, you must have a solid floor. Similarly, to give a solid ground for your data converter circuit, you must use an analog ground plane. This will put your circuit on a solid foundation.

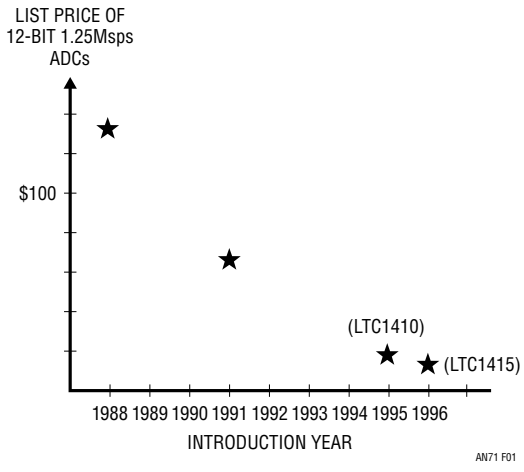


Figure 1. High Performance 1.25Msps, 12-Bit ADCs Are Becoming Affordable to a New Range of Applications. More System Designers Will Need to Know How to Use Them Effectively

Figure 2 shows grounding techniques for the LTC1410, a 1.25Msps, 12-bit ADC. This provides an example that can be modified for the particular high performance converter used. All bypass caps, reference caps and ground connections for the ADC should be tied to the analog ground plane. Tie them as close together as possible to reduce the sensitivity to currents that may flow in the ground plane. The input signal circuitry, filter caps and op amp bypass caps (not shown) should also be grounded to the ground plane near the ADC.

Noise from digital components in the system must be kept out of the analog ground. To do this, boards should be designed with separate analog and digital ground planes, as shown in Figure 2. (The figure shows a 2-layer board layout. If more layers are available, separate layers may be used for analog and digital ground planes.) All noisy digital logic devices must be on the digital ground plane. All the grounds and bypass caps of the ADC (even the digital ones) should tie to the analog ground plane. Tie the two ground planes together at only one point to keep digital currents from taking shortcuts through the analog ground. In single ADC systems this connection can be made at the ADC's digital output driver ground pin (or the digital ground pin). In systems with more than one ADC, this cannot be done without creating more than one tie point between the ground planes. In this case, a different connection point can be used (for example, at the power supply). In any case, be sure to use only a single connection point.

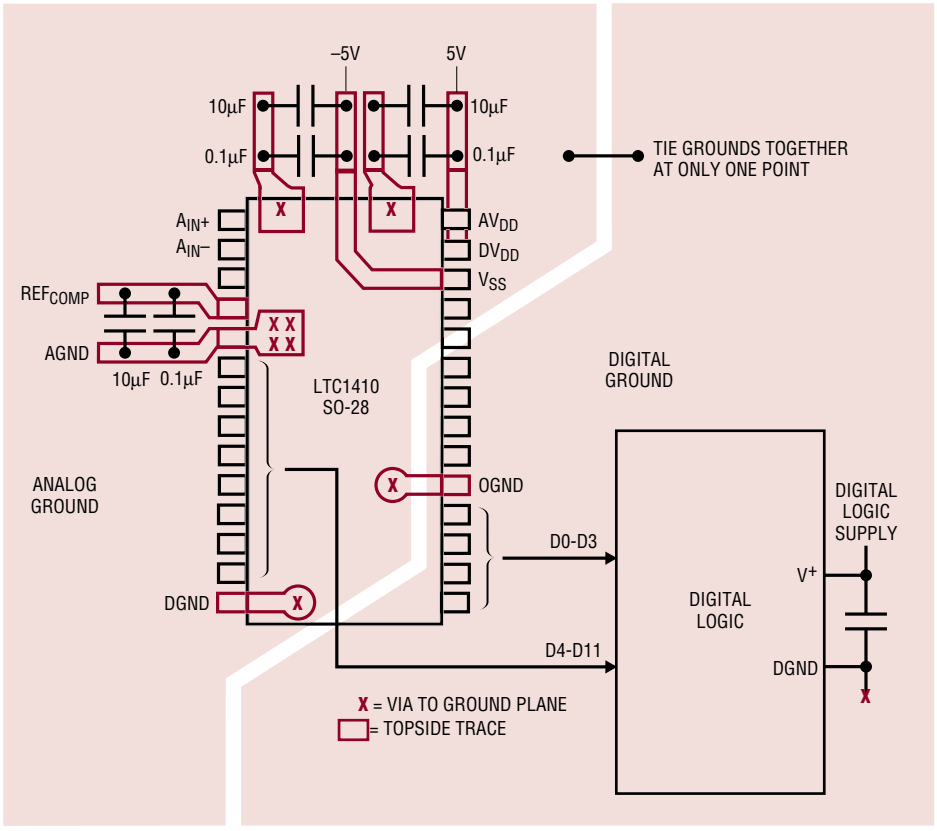


Figure 2. High Performance ADC Layout Must Have Separate Analog and Digital Ground Planes, Bypass Caps with Short Connections and Digital Outputs Routed Away from the Inputs

SUPPLY BYPASSING

The high conversion rates of high performance converters require proper bypassing on the supply pins. The key to good bypassing is low lead inductance between the ADC and the bypass capacitors. The goal is to force AC currents to flow in the shortest possible loop from the supply pin through the bypass cap and back through ground to the ground pin.

In Figure 2, the first components placed around the ADC are the bypass caps, which are located as close as possible to the supply pins. The capacitors must have low inductance and low equivalent series resistance (ESR). Tantalum 10µF surface mount devices are good if they are used in conjunction with 0.1µF ceramics. Even better are the new surface mount ceramic capacitors (e.g., Murata, 1210 sized, 10µF/16V units), which can be used alone. They come in values of 10µF or more and have ESR values as low as 20m .

Figure 3a shows the differential nonlinearity (DNL) of the LTC1410 with good supply bypassing. Figure 3b shows the effects of 2 inches of lead length (corresponding to roughly 60nH of inductance) in series with the supply bypass caps. This is an exaggerated case of poor bypassing layout, which causes the DNL to degrade beyond 1LSB, reducing the accuracy to 11 bits. For best performance, use supply bypass leads of less than one-half inch. A little care pays off with excellent performance (Figure 3a).

REFERENCE BYPASSING

The ADC's analog reference input provides the scale factor for the conversion. For a clean data output the reference must be noise free. Dynamic currents pulled from the reference by the ADC as it converts perturb the reference unless it is properly bypassed. Surface mount tantalum or ceramic capacitors provide good results. hey should be located near the reference pin and should be grounded very near the ADC analog ground pin, as shown in Figure 2.

Figure 3c shows the easily recognizable signature of a reference bypassing problem—a bow-tie shape to the error curve. This occurs because reference perturbations feed in with full strength for inputs near plus or minus full scale but have less effect for inputs near zero scale. This

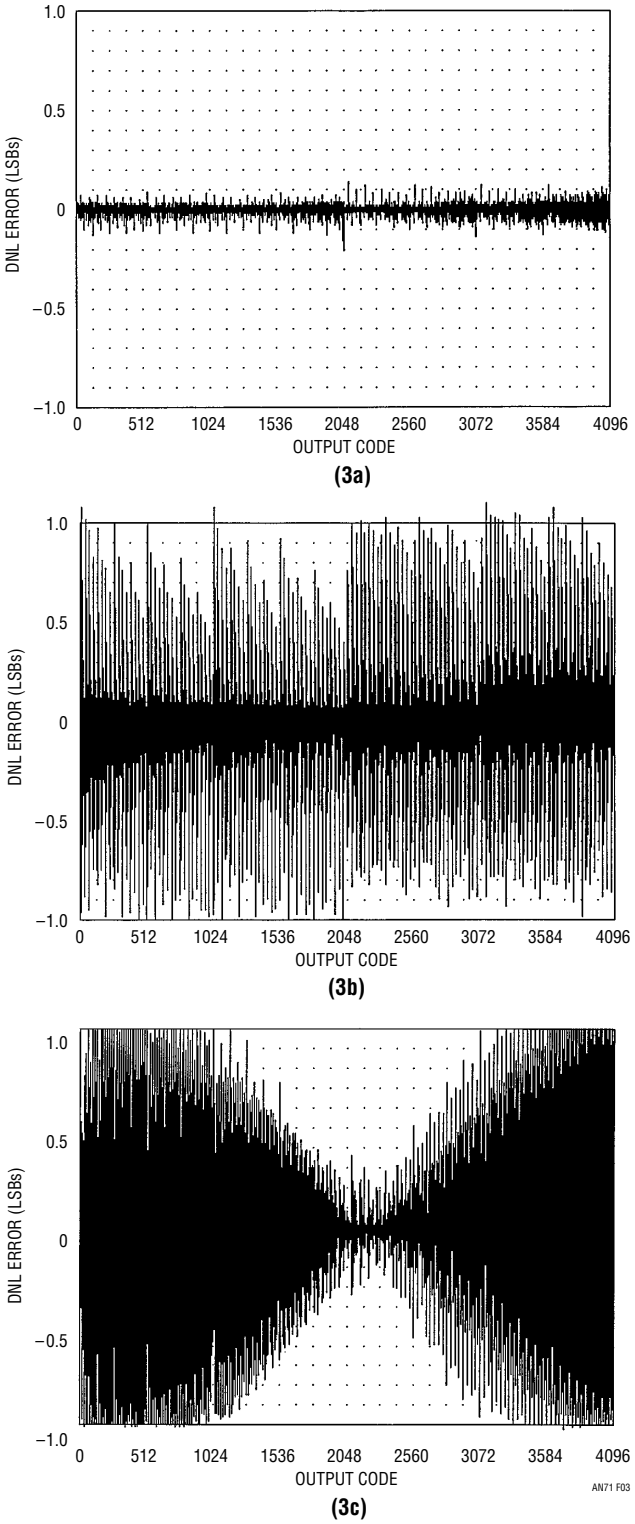


Figure 3. Poor Layout Will Degrade the Differential Nonlinearity (DNL) of Fast ADCs: (a) a Clean LTC1410 Layout with Bypass Cap Wires of Less than 0.5 Inch; (b) 2-Inch Wires to Supply-Bypass Caps;(c) a Wire of More than 2 Inches to the Reference-Bypass Cap

degradation in DNL results from several inches of lead length in series with the reference bypass caps. Once again, this is an exaggerated case to make the consequences of poor bypassing more visible. To maintain high accuracy, keep the lead lengths less than half an inch (Figure 3a).

DRIVING THE ANALOG INPUT

Switched Capacitor Inputs

The inputs to switched capacitor ADCs are easy to drive if you allow for the fact that they draw a small input-current transient at the end of each conversion. This happens when the internal sampling capacitors switch back onto the input to acquire the next sample. For accurate results, the circuitry driving the analog input must settle from this transient before the next conversion is started.

There are two ways to accomplish this. One is to drive the ADC with an op amp that settles from a load transient in less than the acquisition time of the ADC. Fortunately, most op amps settle much more quickly from a load transient than from an input step, so meeting this requirement is not too difficult. The LT1363, for example, is a good choice for driving the LTC1410 input.

A second solution to handling the input transient is to use an input RC filter with a capacitor much larger than the ADC input capacitance. This larger capacitor provides the charge for the sampling capacitor, which eliminates the voltage transient altogether. Figure 4 shows such a filter for the LTC1410. The 1000pF capacitor provides the input charge for the ADC's sampling capacitor. The LT1363's capacitive load driving capability makes it a good choice for use with this filter.

Filtering Wideband Noise from the Input Signal

Many new converters have wide S/H input bandwidths. This is great for capturing high frequency input signals, but for lower input bandwidth applications the converter will pick up any wideband noise that may be in the input signal. To avoid this, use a filter at the ADC input to pass only your desired signal bandwidth.

The simple filter in Figure 4 bandlimits the input signal to 3MHz and still allows clean sampling up to the Nyquist frequency (625kHz). Figure 7a shows the Nyquist performance of the LTC1410 using this filter. The signal to noise and distortion ratio (SINAD) is 71.5dB and total harmonic distortion (THD) is –84dB.

Choosing an Op Amp

To drive high performance ADCs, you will need a high performance op amp.

The noise and distortion of good ADCs are now so low that they no longer mask the performance of the op amp. This adds another tradeoff to op amp selection.

High speed, current feedback op amps have lower DC precision and don't settle as well to high accuracy (for example, 0.01%) as the voltage feedback types. However,

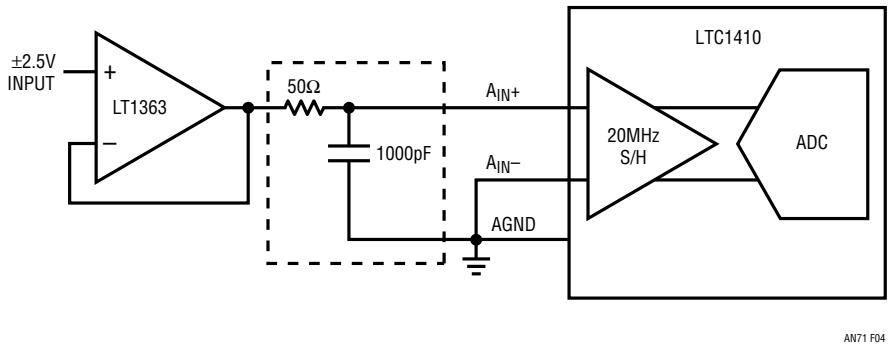
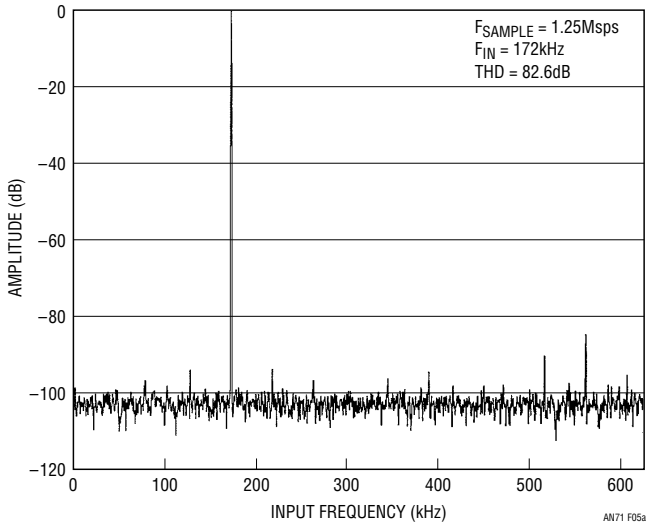


Figure 4. Many New ADCs Have Wide Bandwidth Sample-and-Holds. In Lower Bandwidth Applications, a Simple RC Filter Will Remove Wideband Noise that May Be Present in the Input Signal

they have the best distortion and drive for high speed AC frequency domain applications. Figure 5a shows the FFT result of an LT1227 current feedback amp driving a 172kHz signal into the LTC1410. The distortion (THD) of –82dB is about 3dB worse than the –85dB of the ADC alone.

High speed voltage feedback amplifiers have better precision and settling. They work well in frequency domain applications but are best suited for high speed, time domain or multiplexed applications where their DC precision and settling are required. Figure 5b shows the voltage feedback LT1363's 2dB further degradation in distortion (to –80dB) under the same conditions.

Slower op amps like the OP-27/OP-37 are excellent in noise and precision but are simply not fast enough for high frequency applications. They distort as they are pushed beyond their slewing capabilities (as shown in the FFT plot of Figure 5c).



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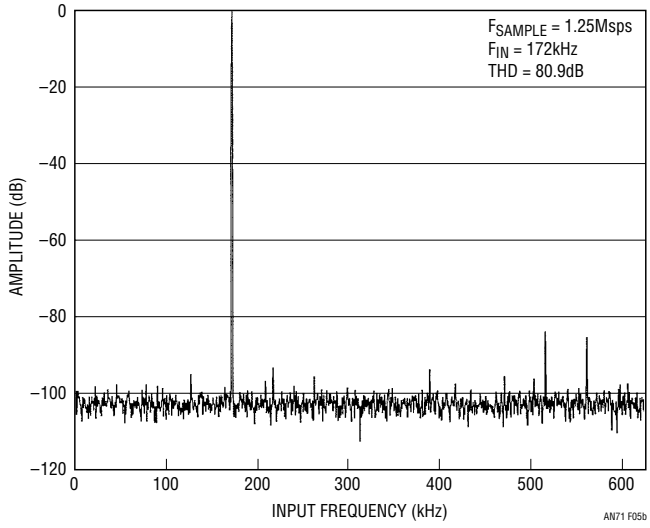

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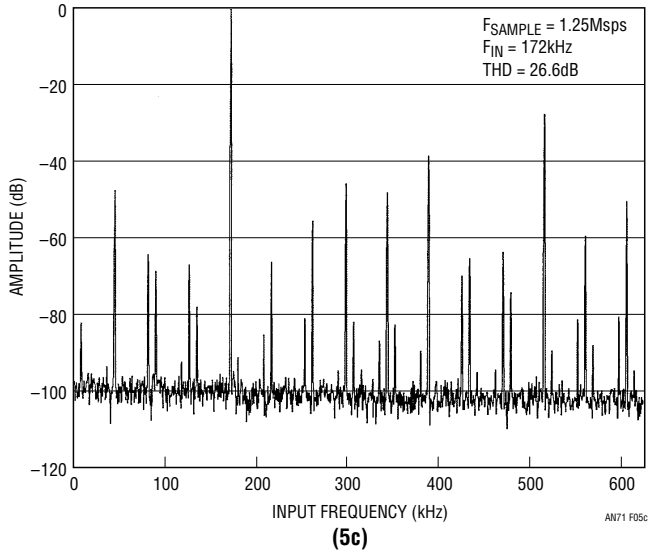


(5c)

Figure 5. Op Amp Selection is Important When an ADC Has Low Distortion Levels. (a) Current Feedback Op Amps Such as the LT1227 (Seen Here Driving the LTC1410) Provide the Lowest THD in the FFT Output; (b) Fast Voltage Feedback Op Amps Do Nearly as Well in THD as Current Feedback Amps and Offer Better Precision; (c) Slower Op Amps Pushed Beyond Their Slew Limits Will Severely Distort Fast Signals

DRIVING THE CONVERT-START INPUT

An improperly driven conversion-start input can create conversion errors in a couple of ways. First, if an ADC has internal timing, the returning edge of the convert signal (the opposite edge from the one that starts the conversion) can couple noise into the converter if it occurs during the conversion time. To avoid this, use a narrow pulse for convert-start instead of a square wave. This ensures that it either returns quickly (after the sample is taken but before the conversion gets underway), or returns after the conversion is over. (This does not apply to those ADCs that draw all their timing from a clock input and require precise 50% duty-cycle clock inputs.)

A convert-start signal that overshoots or rings can also degrade performance. If it overshoots beyond the supply rails it can turn on the ADC's input protection diodes and couple noise into the converter. If it rings, it may still be bouncing around as the ADC's sample-and-hold captures the input signal, which can affect the conversion result. Normally, overshoot and ringing are not a problem with CMOS logic on a well designed board but they are still things to watch out for.

Effects of Jitter

High frequency or high slew rate input signals impose another requirement on the ADC: low aperture jitter. Aperture jitter is the variation in the ADC's aperture delay from conversion to conversion and results in an uncertainty in the time when the input sample is taken. Figure 6 shows how this jitter causes an equivalent input noise by working against the slew rate of the analog input signal. The faster the input signal slew rate, the worse the noise for a given jitter. The best possible SINAD for an ADC is limited by the jitter according to the formula:

$$SINAD(dB) \quad 20\log[1/(2 \bullet t_{JITTER(RMS)} \bullet f_{INPUT})]$$

where:

$t_{JITTER(RMS)}$ = the RMS jitter in seconds
f_{INPUT} = the analog input frequency in Hz.

The LTC1410's 5ps (RMS) aperture jitter allows clean sampling of inputs far beyond the Nyquist frequency. However, to achieve this performance, the convert-start input signal applied to the ADC must also have low jitter. Figure 7a shows the ADC, driven from a low jitter source, capturing a 600kHz input with 71.5dB SINAD. As Figure 7b shows, adding 70ps of jitter to the conversion-start input signal will raise the noise floor, and reduce the SINAD, by 3dB.

If generating a lower jitter signal is a problem, one trick is to start with a higher frequency clock, which will usually have lower jitter, and then divide the frequency down with fast logic (which retains the lower jitter) to get the desired sample clock frequency.

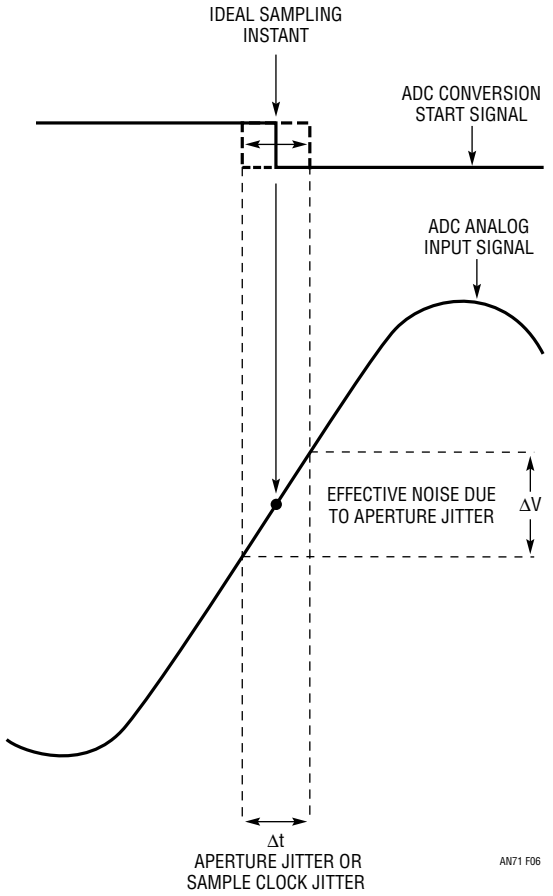


Figure 6. Aperture Jitter in a Sampling ADC or Jitter in the Conversion-Start Signal Applied to the ADC Can Degrade Its Noise Performance. The Time Jitter Works Against the Slope of the Analog Input Signal to Generate an Effective Noise Voltage that Appears in the ADC's Output Spectrum

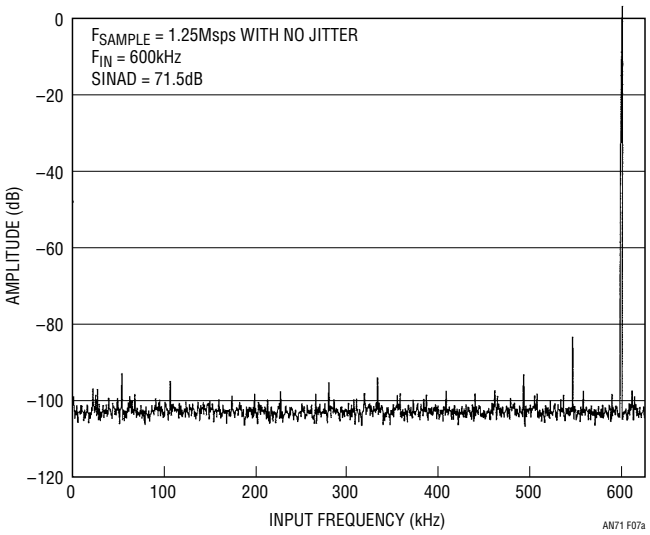
ROUTING THE DATA OUTPUTS

One of the worst potential sources of digital noise and coupling in an ADC is its output data bus. Fortunately, the user can control this with proper board layout. First, to prevent the data outputs of the ADC from capacitively coupling to the analog input circuitry, they should be routed in the opposite direction. This will tend to occur naturally if separate digital and analog ground plane layouts are used, as in Figure 2. Second, the digital output drivers in the ADC switch quickly and will create large current transients if they are loaded with too much capacitance. Locating the receiving buffers or latches close to the ADC will minimize this loading.

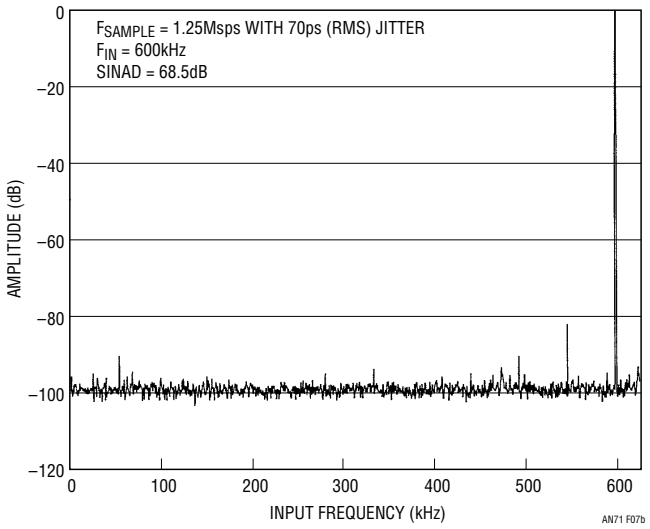
Although reduced, some capacitive currents still flow, and it is important to control their return path to the driver of the ADC. Starting from the output drivers of the ADC, the current goes through the output lines, charges the input capacitance of the receiving latches or buffers, and returns through the digital ground plane to the ADC's output driver. For a falling edge, this current returns into the output driver ground pin. For a rising edge, it returns to the ground point of the output driver's supply-bypass cap. Tying the digital and analog grounds together at the ADC output driver ground pin (as in Figure 2) helps prevent this current from flowing across the analog ground plane. If the grounds must be tied at the power supply instead of at the ADC, the return currents will flow through the analog ground plane. In this case, it is especially important to minimize these currents by minimizing the capacitive loading on the digital outputs.

CONCLUSION

With attention to these principles of layout and design, the new generation of high speed ADCs will provide excellent results. The new devices provide cleaner signal capture than older devices at affordable prices. It makes sense to get all the performance you can.



(7a)

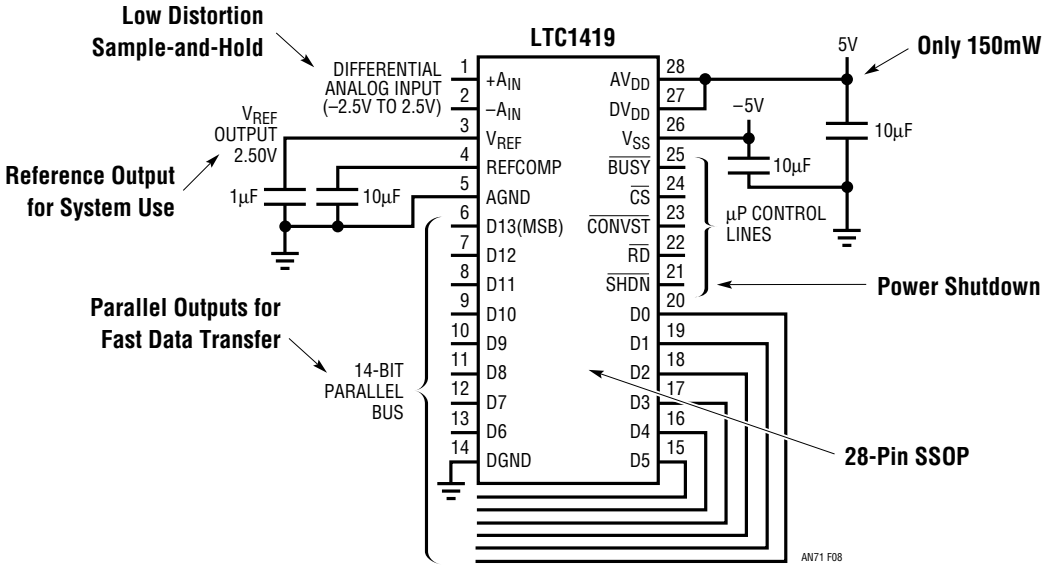


(7b)

Figure 7. Jitter in the Conversion Start Signal Creates Noise: (a) with a Low Jitter Source, the LTC1410 Will Give 71.5dB SINAD when Sampling a Nyquist Input Signal; (b) Adding 70ps of Jitter to the Convert-Start Signal Will Raise the Noise Floor by 3dB to 68.5dB

HIGH SPEED A/D CONVERTERS — World's Best Power/Speed Ratio

Low Power 800kHz, 14-Bit Sampling ADC



Family Features

- Up to 3Msps (LTC1412)
- 12-Bit to 16-Bit Resolution
- ±5V or 5V Supply Operation
- High Bandwidth Sample-and-Holds
- Excellent SINAD at Nyquist
- Surface Mount Packages (SSOP)
- Nap and Sleep Modes
- Internal References

PART NUMBER	RESOLUTION	SPEED	COMMENTS	DATABOOK
16-Bit				
LTC1604	16	333ksps	±2.5V Input Range, ±5V Supply	New
LTC1605	16	100ksps	±10V Input Range, Single 5V Supply	New
14-Bit				
LTC1414	14	2.2Msps	150mW, 81.5dB SINAD and 95dB SFDR	New
LTC1419	14	800ksps	150mW, 81.5dB SINAD and 95dB SFDR	New
LTC1416	14	400ksps	75mW, Low Power with Excellent AC Specs	New
LTC1418	14	200ksps	15mW, Single 5V, Serial/Parallel I/O	New
12-Bit				
LTC1412	12	3Msps	150mW, 71.5dB SINAD and 84dB THD	New
LTC1410	12	1.25Msps	150mW, 71.5dB SINAD and 84dB THD	**96** 6-58
LTC1415	12	1.25Msps	55mW, Single 5V Supply	**96** 6-73
LTC1409	12	800ksps	80mW, 71.5dB SINAD and 84dB THD	**96** 6-47
LTC1279	12	600ksps	60mW, Single 5V or ±5V Supply	**95** 6-8
LTC1278-5	12	500ksps	75mW, Single 5V or ±5V Supply	**94** 6-80
LTC1278-4	12	400ksps	75mW, Single 5V or ±5V Supply	**94** 6-80
LTC1400	12	400ksps	High Speed Serial I/O in SO-8 Package	**96** 6-36

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